40G QSFP+ SR4 Transceiver
Hot Pluggable, MPO/MTP, 850nm VCSEL, Multi-Mode, 100M, DDM

Part number: SQ85D0-X1ATOZ

Overview:

SQ85D0-X1ATOZ is a parallel fiber optical transceiver module for 40Gbit/s data transmission applications at 850nm. It is ideally suited for 40GbE datacom & storage area network(SAN/NAS) applications based on the IEEE 802.3ba 40GBase-SR4 standard. Designed for short range multi-lane data communication and integrates four independent transmit and receive channels. Each capable 10Gbps operation for an aggregate data rate of 40Gbps over 100 meters using OM3 multi mode fiber. An optical fiber cable with an MPO/MTP™ connector can be plugged into the QSFP+ module receptacle.

Applications:

- 40GBASE-SR4 Ethernet
- Data Center
- Datacom/ Telecom Switch & Router
- Infiniband QDR, DDR and SDR

Features:

- Compliant to SFF-8436 QSFP+ MSA
- 4 independent full-duplex channels
- Up to 11.2Gbps data rate per channel
- Link length up to 100m over MM OM3 fiber and 150m over MM OM4 fiber
- 850nm VCSEL array transmitter
- MPO/MTP™ optical connector
- Built-in digital diagnostic function
- Single 3.3V power supply
- Power level 1: Max. power <1.5W
- RoHS compliant

Absolute Maximum Ratings :

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-20	+85	°C
Storage Relative Humidity	RH	5	85	%
Supply Voltage	V_{cc3}	-0.5	+3.6	V

Recommended Operating Conditions :

Parameters	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{cc}	+3.135	+3.3	+3.465	V
Supply Current	I_{cc}			350	mA
Module Total Power	P			1.5	W

Transmitter Electro-optical Characteristics :

V_{CC}= 3.135V to 3.465V, T_{OP} = 0 °C to 70 °C

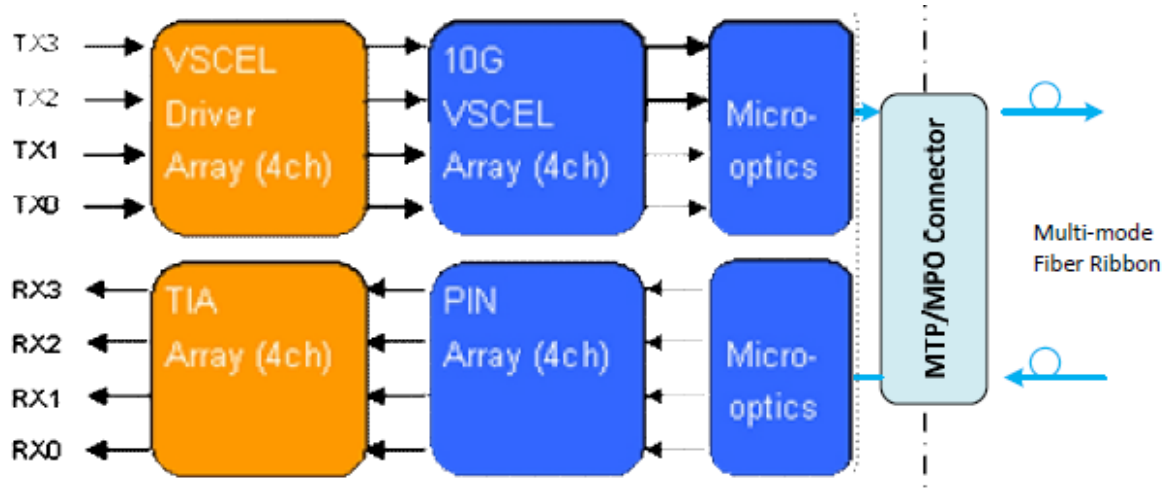
Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Date Rate	DR		10.3125	11.2	Gb/s	
Bit Error Rate	BER			10^{-12}		
Average Optical Power, each Lane	P_{AVG}	-7.6		+2.4	dBm	
Optical Modulation Amplitude (OMA)	P_{OMA}	-5.6		+3	dBm	
Optical Wavelength	λ	840	850	860	nm	
Spectral Width (RMS)	△λ			0.65	nm	
Optical Extinction Ratio	ER	3			dB	
Average Optical Power of OFF transmitter, each Lane				-30	dBm	
Optical Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.23, 0.34, 0.43, 0.27, 0.33, 0.4}				
Average Launch Power OFF, each Lane	P_{OFF}			-30	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance				12	dB	
Input differential impedance	Rid	80	100	120	Ω	
Differential data input voltage	V_{DIFF}	90		1600	mV	
Control I/O Voltage, High	V_{IH}	2.0		Vcc	V	
Control I/O Voltage, Low	V_{IL}	GND		GND+0.7	V	

Receiver Electro-optical Characteristics :

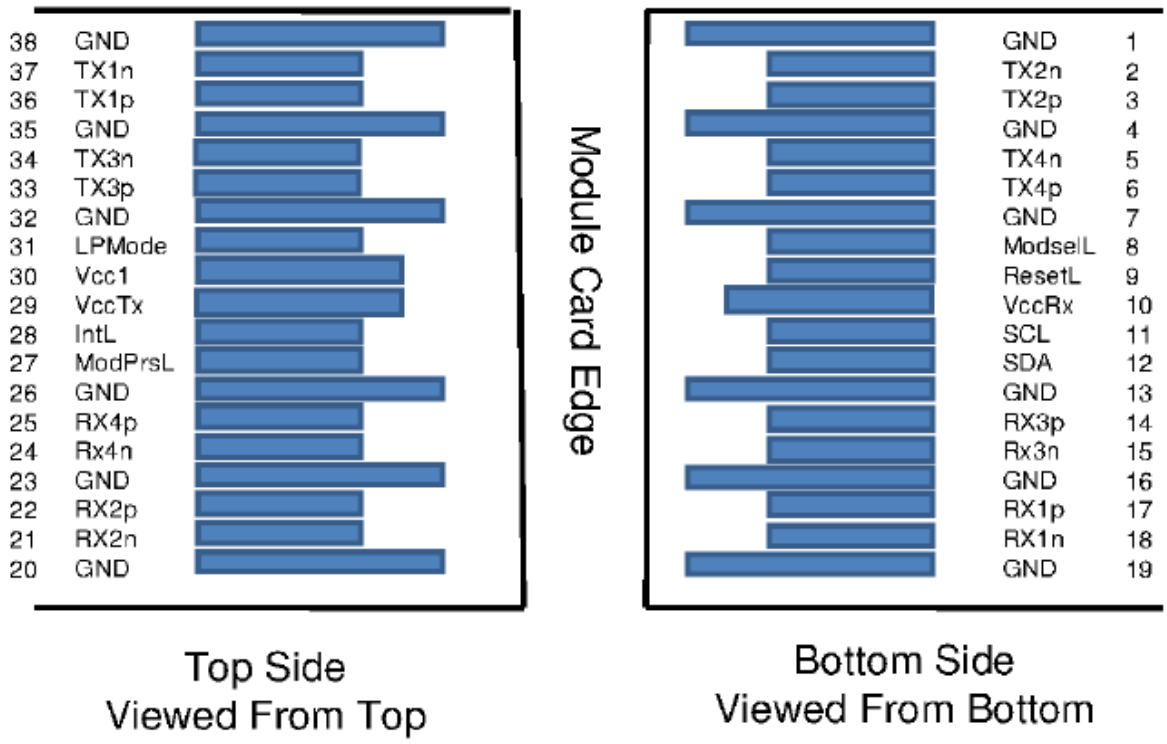
V_{CC}= 3.135V to 3.465V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Date Rate	DR		10.3125	11.2	Gb/s	
Damage Threshold	D_{TH}	+3.4			dBm	
Average Receiver Input Power	P_{IN_AVG}	-9.5		+2.4	dBm	
Receiver Sensitivity (OMA), each Lane	P_{IN_sen}			-10	dBm	
Stressed Receiver Sensitivity (OMA), each Lane	$P_{IN\_s\text{-}oma}$			-5.4	dBm	
Optical Center Wavelength	λ_C	840	850	860	nm	
LOS De-Assert	LOS_D			-13	dBm	
LOS Assert	LOS_A	-30		-16	dBm	
LOS Hysteresis	LOS_{HY}	0.5			dB	
Differential data output voltage	Vout,pp		600	800	mV	

Transceiver Block Diagram:



Pin Assignment :



Pin Description :

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output

15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2p	Receiver Non-Inverted Data Output
22	CML-O	Rx2n	Receiver Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4p	Receiver Non-Inverted Data Output
25	CML-O	Rx4n	Receiver Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMode	Low Power Mode
32		GND	Module Ground
33	CML-I	Tx3n	Transmitter Inverted Data Input
34	CML-I	Tx3p	Transmitter Non-Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1n	Transmitter Inverted Data Input
37	CML-I	Tx1p	Transmitter Non-Inverted Data Input
38		GND	Module Ground

Note1: GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and ransmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Digital Diagnostic Functions :

As defined by the QSFP+ MSA , Sanoc's QSFP+ transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

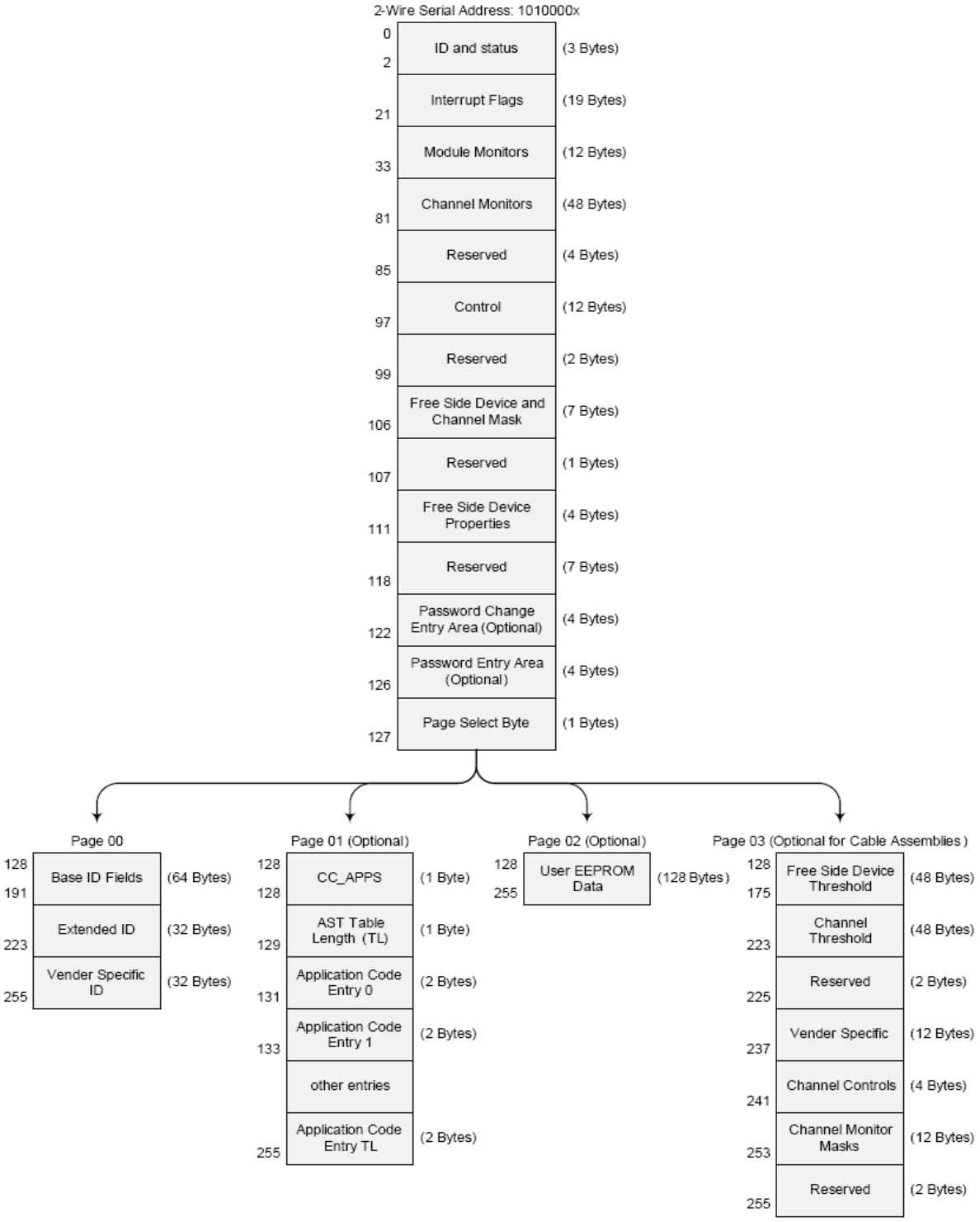
- Transceiver temperature
- Laser bias current (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

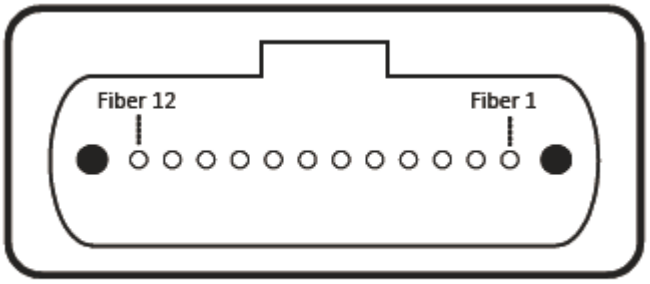
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP+ transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP+ transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP+ MSA Specification.

QSFP+ and Digital Diagnostic Memory Map



Optical Interface Lanes and Assignment

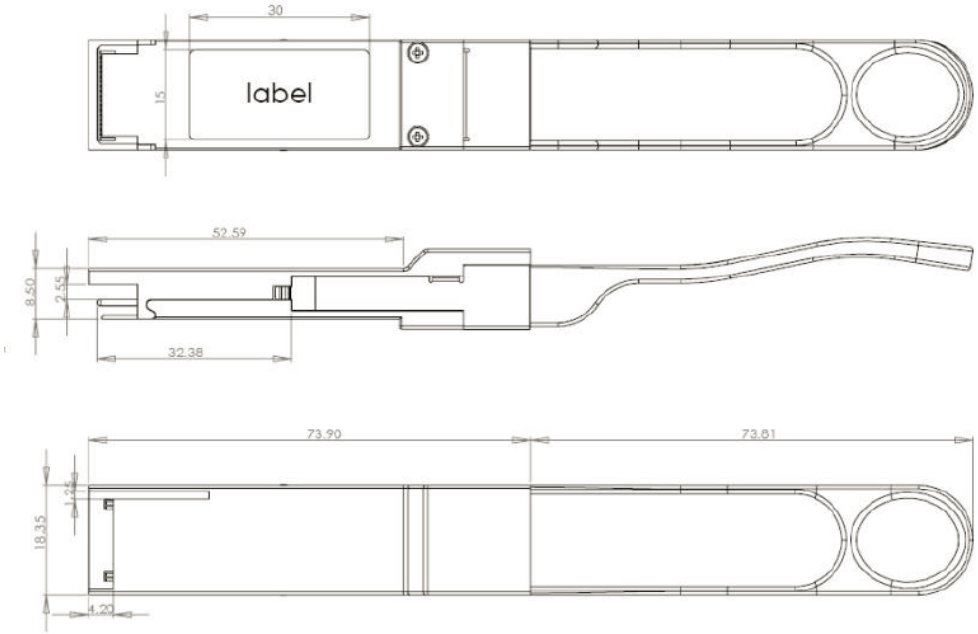


Outside view of the QSFP module MPO

Fiber #	Lane Assignment
1	RX0
2	RX1
3	RX2
4	RX3
5,6,7,8	Not used
9	TX3
10	TX2
11	TX1
12	TX0

lane assignment

Mechanical Dimensions :



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information :

Part No.	TX	Link	DDM	Temp.
SQ85D0-X1ATOZ	850nm	100m/ OM3	Yes	0~70°C