40G QSFP+ LR4 Transceiver
Hot Pluggable, Duplex LC, 1310nm CWDM LD, Single Mode, 10KM, DDM

Part number: SQ13D0-10ATOZ

Overview:

SQ13D0-10ATOZ is a parallel fiber optical transceiver module for 40Gbit/s data transmission applications at 1310nm CWDM. It is ideally suited for 40GbE datacom & Storage area network (SAN/NAS) applications based on the IEEE 802.3ba 40GBase Ethernet standard.
The transceiver incorporates a 4-channel laser driver circuit together with a 4-channel DFB array coupled with an optical multiplexer. On the receiver side, an optical de-multiplexer is coupled with a 4-channel photodiode array and a 4-channel TIA array resulting in a compact transceiver module for an aggregate bandwidth of 40Gb/s .

Applications:

- 40GBASE-LR4 Ethernet
- Data Center
- Datacom/ Telecom Switch & Router
- Infiniband QDR and DDR

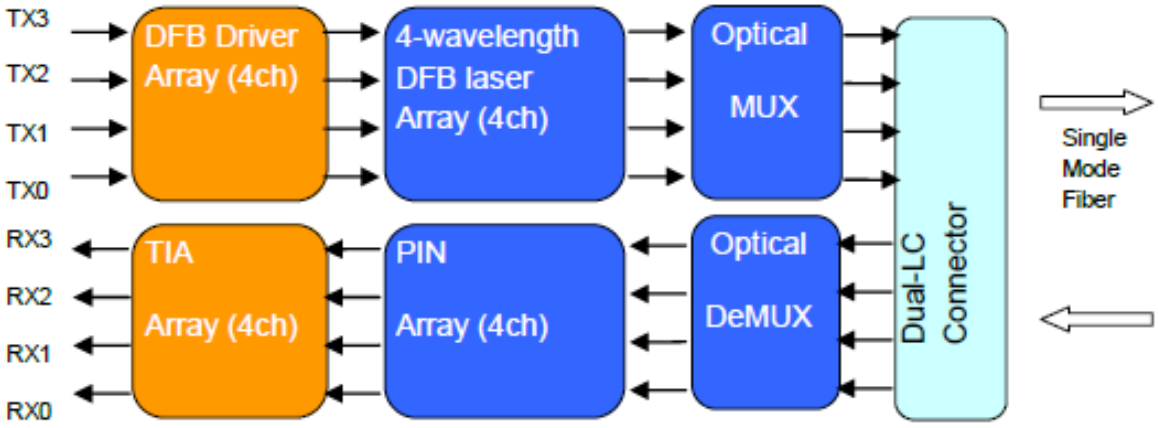
Features:

- Compliant to SFF-8436 QSFP+ MSA
- Compliant to IEEE802.3ba 40GBase-LR4
- Compliant with QDR/DDR infiniband data rates
- 4-CH CWDM lanes Mux/DeMux design
- Up to 11.2Gbps data rate per CWDM lane
- Link length up to 10km over single mode fiber
- 1310nm CWDM DFB array transmitter
- Duplex LC connector
- Built-in digital diagnostic function
- Single 3.3V power supply
- Max. power <3.5W
- RoHS compliant

Absolute Maximum Ratings :

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-20	+85	°C
Storage Relative Humidity	RH	5	85	%
Supply Voltage	V_{cc3}	-0.5	+3.6	V

Transceiver Block Diagram:



Recommended Operating Conditions :

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{cc}	+3.135	+3.3	+3.465	V
Supply Current	I_{cc}			960	mA
Module Total Power	P			3.5	W

Transmitter Electro-optical Characteristics :

V_{CC}= 3.135V to 3.465V, T_{OP} = 0 °C to 70 °C

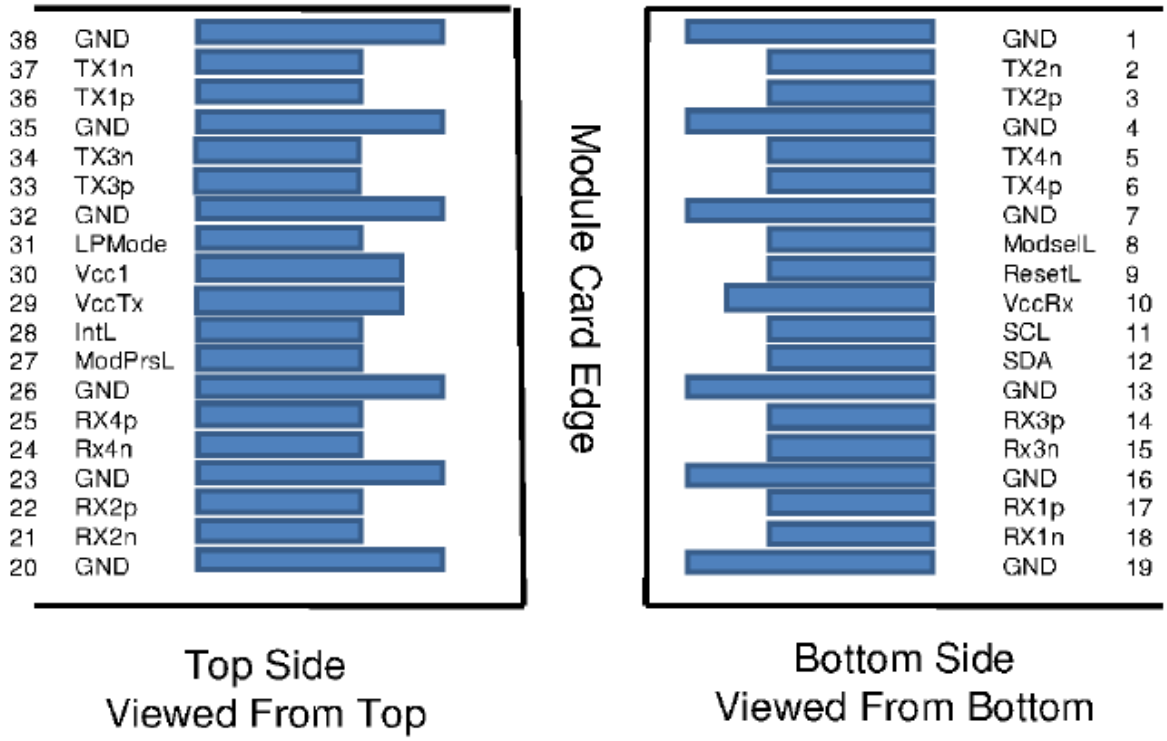
Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Date Rate, each Lane	DR		10.3125	11.2	Gb/s	
Bit Error Rate	BER			10^{-12}		
Total Average Optical Launch Power	P_{T-AVG}			+8.3	dBm	
Average Launch Power, each Lane	P_{AVG}	-7.0		+2.3	dBm	
Optical Modulation Amplitude(OMA), each lane	P_{OMA}	-4.0		+3.5	dBm	
Launch Power in OMA minus Transmitter and Dispersion Penalty, each Lane	P_{TP}	-4.8			dB	
Dispersion Penalty, each Lane	TDP			2.3	dB	
Difference in Launch Power between any two Lanes (OMA)				6.5	dB	
Optical Wavelength	λ_{L0}	1264.5	1271	1277.5	nm	
	λ_{L1}	1284.5	1291	1297.5	nm	
	λ_{L2}	1304.5	1311	1317.5	nm	
	λ_{L3}	1324.5	1331	1337.5	nm	
Spectral Width (-20dB)	$\triangle\lambda$			1	nm	
Optical Extinction Ratio	ER	3.5			dB	
Optical Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Average Launch Power OFF, each Lane	P_{OFF}			-30	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance				20	dB	
Transmitter Reflectance				-12	dB	
Input differential impedance	Rid	85	100	115	Ω	
Differential data input voltage	V_{DIFF}	150		1200	mV	
Control I/O Voltage, High	V_{IH}	2.0		Vcc	V	
Control I/O Voltage, Low	V_{IL}	GND		GND+0.7	V	

Receiver Electro-optical Characteristics :

V_{CC}= 3.135V to 3.465V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Date Rate, each Lane	DR		10.3125	11.2	Gb/s	
Damage Threshold	D_{TH}	+3.3			dBm	
Average Power at Receiver Input, each Lane	P_{IN_avg}	-13.7		+2.3	dBm	
Receiver Power (OMA), each Lane				+3.5	dBm	
Stressed Receiver Sensitivity in OMA, Each Lane				-9.9	dBm	
Receiver Sensitivity, each Lane	P_{IN_sen}		-	-11.5	dBm	
Difference in Receive Power between any two Lanes (OMA)				7.5	dB	
Optical Center Wavelength	λ_C	1260		1600	nm	
Receiver Reflectance	Rrx			-26	dB	
LOS De-Assert	LOS_D			-12	dBm	
LOS Assert	LOS_A	-20			dBm	
LOS Hysteresis	LOS_{HY}	1			dB	
Differential data output voltage	Vout,pp	370		950	mV	

Pin Assignment :



Pin Description :

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground

14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2p	Receiver Non-Inverted Data Output
22	CML-O	Rx2n	Receiver Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4p	Receiver Non-Inverted Data Output
25	CML-O	Rx4n	Receiver Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMode	Low Power Mode
32		GND	Module Ground
33	CML-I	Tx3n	Transmitter Inverted Data Input
34	CML-I	Tx3p	Transmitter Non-Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1n	Transmitter Inverted Data Input
37	CML-I	Tx1p	Transmitter Non-Inverted Data Input
38		GND	Module Ground

Note1: GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and ransmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Digital Diagnostic Functions :

As defined by the QSFP+ MSA , Sanoc's QSFP+ transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

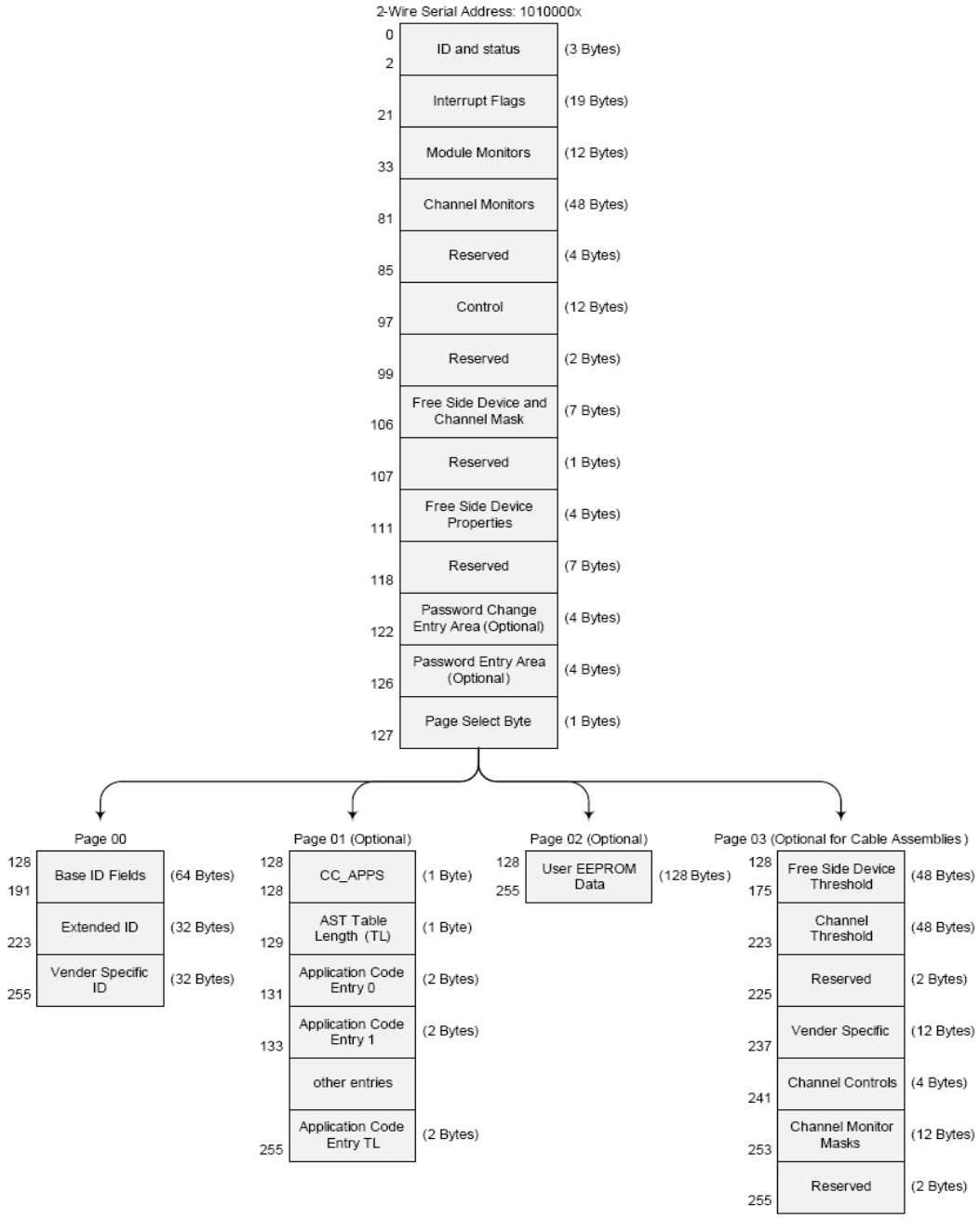
- Transceiver temperature
- Laser bias current (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

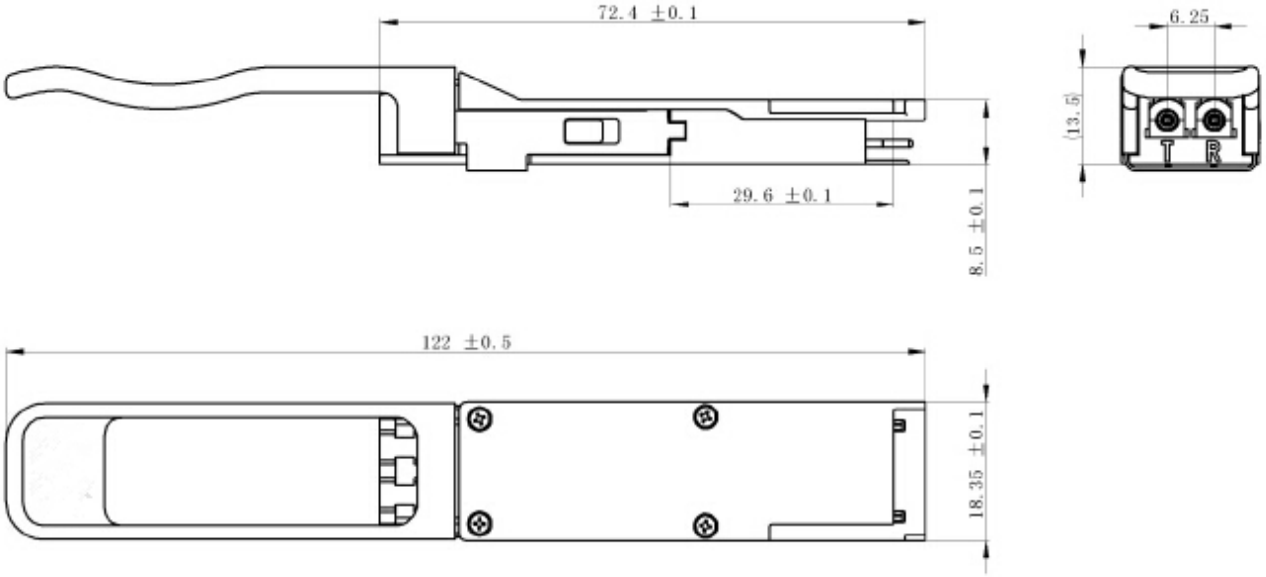
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP+ transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP+ transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP+ MSA Specification.

QSFP+ and Digital Diagnostic Memory Map



Mechanical Dimensions :



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information :

Part No.	TX	Link	DDM	Temp.
SQ13D0-10ATOZ	1271 nm 1291 nm 1311 nm 1331 nm	10km	Yes	0~70°C